In The Claims:

Claims 1-156 (canceled)

157. (original) The process for fabricating a chip structure, comprising:

Step 1: providing a wafer with a plurality of electric devices, an interconnection scheme and a passivation layer, the electric devices and the interconnection scheme arranged inside the wafer, the interconnection scheme electrically connected with the electric devices, the passivation layer disposed on a surface layer of the wafer, the passivation layer having at least one opening exposing the interconnection scheme, wherein the largest width of the opening of the passivation ranges from 0.5 microns to 20 microns;

Step 2: forming a conductive layer over the passivation layer of the wafer, and the conductive layer electrically connected with the interconnection scheme;

Step 3: forming a photoresist onto the conductive layer, and the photoresist having at least one opening exposing the conductive layer;

Step 4: filling at least one conductive metal into the opening of the photoresist, and the conductive metal disposed over the conductive layer;

Step 5: removing the photoresist; and

Step 6: removing the conductive layer not covered with the conductive metal.

158. (original) The process according to claim 157, wherein a dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal after step 6 is performed.

159. (original) The process according to claim 158, wherein at least one node opening is formed through the dielectric sub-layer to expose the conductive metal formed at a lower portion after the dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal.

160. (original) The process according to claim 158, wherein the dielectric sub-layer is made of an organic compound.

161. (original) The process according to claim 158, wherein the dielectric sub-layer is made of a macromolecule polymer.

162. (original) The process according to claim 158, wherein the dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

163. (original) The process according to claim 157, wherein the process further comprises:

Step 7: forming a dielectric sub-layer over the passivation layer, the dielectric sub-layer covering the formed conductive metal, and the dielectric sub-layer having at least one opening exposing the conductive metal formed at a lower portion;

Step 8: forming at least other one conductive layer on the dielectric sub-layer and into the opening of the dielectric sub-layer, and the other conductive layer electrically connected with the metal layer exposed by the opening of the dielectric sub-layer;

Step 9: forming a photoresist onto the other conductive layer, and the photoresist having at least one opening exposing the other conductive layer;

Step 10: filling at least other one conductive metal into the opening of the photoresist, and the other conductive metal disposed over the other conductive layer;

Step 11: removing the photoresist; and

Step 12: removing the other conductive layer not covered with the other conductive metal.

164. (original) The process according to claim 163, wherein the dielectric sub-layer is made of an organic compound.

165. (original) The process according to claim 163, wherein the dielectric sub-layer is made of a macromolecule polymer.

166. (original) The process according to claim 163, wherein the dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

167. (original) The process according to claim 163, wherein the thickness of the dielectric sub-layer ranges from 1 micron to 100 microns.

168. (original) The process according to claim 163, wherein at least other one dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal after the step 12 is performed.

169. (original) The process according to claim 168, wherein at least one node opening is formed through the other dielectric sub-layer to expose the conductive metal

formed at a lower portion after the other dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal.

170. (original) The process according to claim 168, wherein the other dielectric sub-layer is made of an organic compound.

171. (original) The process according to claim 168, wherein the other dielectric sub-layer is made of a macromolecule polymer.

172. (original) The process according to claim 168, wherein the other dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

173. (original) The process according to claim 163, wherein the sequential steps 7-12 are repeated at least one time.

174. (original) The process according to claim 173, wherein at least other one dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal after the sequential steps 7-12 are repeated at least one time.

175. (original) The process according to claim 174, wherein at least one node opening is formed through the other dielectric sub-layer to expose the conductive metal formed at a lower portion after the other dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal.

176. (original) The process according to claim 174, wherein the other dielectric sub-layer is made of an organic compound.

177. (original) The process according to claim 174, wherein the other dielectric sub-layer is made of a macromolecule polymer.

178. (original) The process according to claim 174, wherein the other dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

179. (original) The process according to claim 157, wherein the thickness of the trace constructed of the conductive layer and the conductive metal ranges from 1 micron to 50 microns.

180. (original) The process according to claim 157, wherein the width of the trace constructed of the conductive layer and the conductive metal ranges from 1 micron to 1 centimeter.

181. (original) The process according to claim 157, wherein the cross-sectional area of the trace constructed of the conductive layer and the conductive metal ranges from 1 square micron to 0.5 square millimeters.

182. (original) The process according to claim 157, wherein the passivation layer is constructed of an inorganic compound.

183. (original) The process according to claim 157, wherein the passivation layer is constructed of a silicon oxide compound, a silicon nitride compound, phosphosilicate glass (PSG), a silicon oxide nitride compound or a composite formed by laminating the above material.

184. (original) The process according to claim 157, wherein, before the step 2 is performed, a dielectric sub-layer is formed on the passivation layer, the dielectric sub-layer includes at least one via metal opening connecting with the opening of the passivation layer, and, then, when the step 2 is performed, the conductive layer is formed on the dielectric sub-layer, the side wall of the via metal opening, and the interconnection scheme exposed by the opening of the passivation layer.

185. (original) The process according to claim 184, wherein the largest width of the via metal opening is larger than that of the opening of the passivation.

186. (original) The process according to claim 184, wherein the cross-sectional area of the via metal opening ranges from 1 square micron to 10,000 square microns.

187. (original) The process according to claim 157, wherein during the step 2, a sputtering process is used to form the conductive layer over the passivation layer of the wafer.

188. (original) The process according to claim 157, wherein during the step 4, an electroplating process is used to fill the conductive metal over the conductive layer.

189. (original) The process according to claim 157, wherein the material of the conductive layer includes titanium-tungsten alloy, titanium or chromium.

190. (original) The process according to claim 157, wherein the material of the conductive metal includes copper, nickel, or gold.

191. (original) The process for fabricating a chip structure, comprising:

Step 1: providing a wafer with a plurality of electric devices, an interconnection scheme and a passivation layer, both the electric devices and the interconnection scheme arranged inside the wafer, the interconnection scheme electrically connected with the electric devices, the passivation layer disposed on a surface layer of the wafer, the passivation layer having at least one opening exposing the interconnection scheme;

Step 2: forming at least one conductive metal over the passivation layer of the wafer, and the conductive metal electrically connected with the interconnection scheme;

Step 3: forming a photoresist onto the conductive metal, and patterning the photoresist to expose the conductive metal to the outside;

Step 4: removing the conductive metal not covered with the photoresist; and

Step 5: removing the photoresist.

192. (original) The process according to claim 191, wherein a dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal after step 5 is performed.

193. (original) The process according to claim 192, wherein at least one node opening is formed through the dielectric sub-layer to expose the conductive metal formed at a

lower portion after the dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal.

194. (original) The process according to claim 192, wherein the dielectric sub-layer is made of an organic compound.

195. (original) The process according to claim 192, wherein the dielectric sub-layer is made of a macromolecule polymer.

196. (original) The process according to claim 192, wherein the dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

197. (original) The process according to claim 191, wherein a conductive layer, the material of which includes titanium-tungsten alloy, titanium or chromium, is formed over the passivation layer of the wafer before the step 2 is performed, and then the conductive metal is formed on the conductive layer when the step 2 is performed.

198. (original) The process according to claim 197, wherein a sputtering process is used to form the conductive layer over the passivation layer of the wafer.

199. (original) The process according to claim 197, wherein an electroplating process or a sputtering process is used to form the conductive metal on the conductive layer.

200. (original) The process according to claim 191, wherein the process further comprises:

Step 6: forming a dielectric sub-layer over the passivation layer, the dielectric sub-layer covering the formed conductive metal, and the dielectric sub-layer having at least one opening exposing the conductive metal formed at a lower portion;

Step 7: forming at least other one conductive metal over the passivation layer of the wafer, and the other conductive metal electrically connected with the conductive metal formed at a lower portion;

Step 8: forming a photoresist onto the other conductive metal, and patterning the photoresist to expose the other conductive metal to the outside;

Step 9: removing the other conductive metal not covered with the photoresist; and

Step 10: removing the photoresist.

201. (original) The process according to claim 200, wherein the dielectric sub-layer is made of an organic compound.

202. (original) The process according to claim 200, wherein the dielectric sub-layer is made of a macromolecule polymer.

203. (original) The process according to claim 200, wherein the dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

204. (original) The process according to claim 200, wherein the thickness of the dielectric sub-layer ranges from 1 micron to 100 microns.

205. (original) The process according to claim 200, wherein at least other one dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal after the step 10 is performed.

206. (original) The process according to claim 205, wherein at least one node opening is formed through the other dielectric sub-layer to expose the conductive metal formed at a lower portion after the other dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal.

207. (original) The process according to claim 205, wherein the other dielectric sub-layer is made of an organic compound.

208. (original) The process according to claim 205, wherein the other dielectric sub-layer is made of a macromolecule polymer.

209. (original) The process according to claim 205, wherein the other dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

210. (original) The process according to claim 205, wherein a conductive layer is formed onto the dielectric sub-layer before the step 7 is performed, and, then, the conductive metal is formed on the conductive layer when the step 7 is performed.

211. (original) The process according to claim 200, wherein the sequential steps 6-10 are repeated at least one time.

212. (original) The process according to claim 211, wherein at least other one dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal after the sequential steps 6-10 are repeated at least one time.

213. (original) The process according to claim 212, wherein at least one node opening is formed through the other dielectric sub-layer to expose the conductive metal formed at a lower portion after the other dielectric sub-layer is formed over the passivation layer and covers the formed conductive metal.

214. (original) The process according to claim 212, wherein the other dielectric sub-layer is made of an organic compound.

215. (original) The process according to claim 212, wherein the other dielectric sub-layer is made of a macromolecule polymer.

216. (original) The process according to claim 212, wherein the other dielectric sub-layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, or elastomer.

217. (original) The process according to claim 191, wherein the thickness of the trace constructed of the conductive layer and the conductive metal ranges from 1 micron to 50 microns.

218. (original) The process according to claim 191, wherein, before the step 2 is performed, a dielectric sub-layer is formed on the passivation layer, the dielectric sub-layer

includes at least one via metal opening connecting with the opening of the passivation layer, and, then, when the step 2 is performed, the conductive metal is formed on the dielectric sub-layer and into the via metal opening.

219. (original) The process according to claim 218, wherein the largest width of the via metal opening is larger than that of the opening of the passivation.

220. (original) The process according to claim 191, wherein the material of the conductive metal includes aluminum, copper, nickel, or gold.